CLAIMS:

1-22 (cancelled);

23. (new) An integrated circuit (IC) supporting non-electrically-programmable three-dimensional memory (NEP-3DM)-based self-test (NEP-3DMST), comprising:

a substrate circuit, said substrate circuit further comprising a circuit-under-test (CUT) and a peripheral circuit;

an NEP-3DM stacked on said substrate circuit and connected with said peripheral circuit through a plurality of inter-level connecting vias, said NEP-3DM comprising at least an NEP-3DM level;

wherein at least a portion of said NEP-3DM stores at least a portion of test data and/or test-data seeds for said CUT.

24. (new) The IC supporting NEP-3DMST according to claim 23, wherein said NEP-3DM comprises more than one NEP-3DM levels, said NEP-3DM levels being stacked on top of one another.

25. (new) The IC supporting NEP-3DMST according to claim 23, wherein at least a portion of said NEP-3DM is a three-dimensional mask-programmable memory.

26. (new) The IC supporting NEP-3DMST according to claim 23, wherein said substrate circuit further comprises a plurality of test-vector buffers, said test-vector buffers storing at least a portion of said test data and/or test-data seeds.

27. (new) The IC supporting NEP-3DMST according to claim 23, wherein said test data or test-data seeds are downloaded into said CUT in a serial fashion.

28. (new) The IC supporting NEP-3DMST according to claim 23, wherein said test data or test-data seeds are downloaded into said CUT in a parallel fashion.

29. (new) The IC supporting NEP-3DMST according to claim 23, wherein

said CUT comprises a first CUT block and a second CUT block;

said substrate circuit further comprises a first test-vector buffer and a second test-vector buffer, said first test-vector buffer storing at least a portion of test data and/or test-data seeds for said first CUT block, said second test-vector buffer storing at least a portion of test data and/or test-data seeds for said second CUT block.

30. (new) The IC supporting NEP-3DMST according to claim 23, wherein said substrate circuit further comprises a D/A converter, said D/A converter converting at least a portion of said digital test vectors into analog signals.

31. (new) The IC supporting NEP-3DMST according to claim 30, wherein said substrate circuit further comprises an analog comparator.

32. (new) The IC supporting NEP-3DMST according to claim 23, wherein

said test data and/or test-data seeds in said NEP-3DM are compressed test data;

said substrate circuit further comprises a data de-compressor for de-compressing said compressed test data.

33. (new) The IC supporting NEP-3DMST according to claim 23, wherein

said test data and/or test-data seeds in said NEP-3DM are compressed test data;

said substrate circuit further comprises a data compressor for compressing output test vectors.

34. (new) The IC supporting NEP-3DMST according to claim 23, wherein said substrate circuit further comprises a storage block, said storage block storing address information associated with mismatched output test vectors and expected test vectors.

35. (new) The IC supporting NEP-3DMST according to claim 23, wherein said substrate circuit further comprises a multiplexor, the output of said multiplexor being selected from external scan-test input or NEP-3DM input.

36. (new) The IC supporting NEP-3DMST according to claim 23, wherein said substrate circuit further comprises a plurality of parallel-serial test flip-flops (PS-TFF), the output of said PS-TFF being selected from normal data input, external scan-test input, and NEP-3DM input.

37. (new) The IC supporting NEP-3DMST according to claim 23 being a portion of a printed-circuit board (PCB), said PCB further comprising a second IC, at least a portion of said NEP-3DM storing at least a portion of test data and/or test-data seeds for said second IC.